

# UTMC APPLICATION NOTE

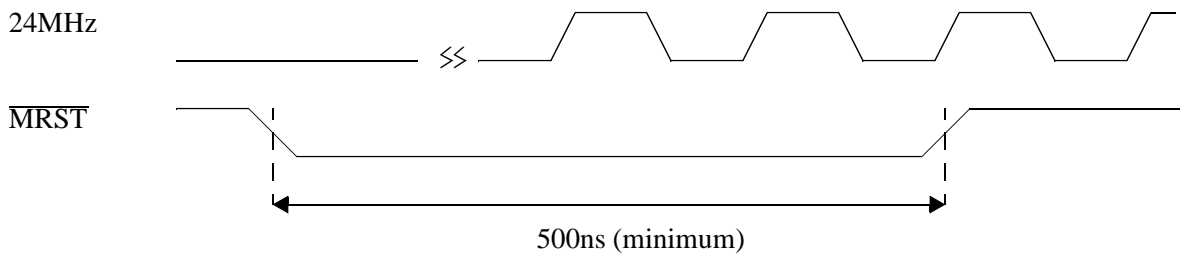
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## UT69151 S $\mu$ MMIT Family: All Revisions

To properly prepare the S $\mu$ MMIT family (i.e., S $\mu$ MMIT, S $\mu$ MMITLX/DX, or S $\mu$ MMIT XT) of devices for operation, assert both master reset ( $\overline{MRST}$ ) and the JTAG reset ( $\overline{TRST}$ ) before attempting device initialization. If not properly reset, the S $\mu$ MMIT family of devices can enter an undefined state and not meet the Date Sheet specifications and required MIL-STD-1553 functionality.

### Master Reset:

Hold input  $\overline{MRST}$  to a logic zero voltage level for at least 500ns while applying a minimum of two 24MHz clocks to input  $24MHz$ . After two 24MHz clock periods and 500ns have passed, input  $\overline{MRST}$  can transition back to a logic one voltage level.



### JTAG Reset:

Hold input  $\overline{TRST}$  to a logical zero voltage level for at least 500ns while applying a minimum of two 24MHz clocks to input  $24MHz$ . For system simplicity, tie  $\overline{TRST}$  to  $\overline{MRST}$ . For systems not using the JTAG port, tie JTAG input  $\overline{TRST}$  to a logic zero voltage level.