

## UTMC APPLICATION NOTE

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### ŞµMMIT XT™ to UT69RH051 Microcontroller

#### Introduction

The monolithic CMOS UT69151 ŞµMMIT provides the system designer with an intelligent solution to MIL-STD-1553 multiplexed serial data bus design problems. The ŞµMMIT is a single-chip device that implements all three of the defined MIL-STD-1553 functions - Remote Terminal, Bus Controller, and Monitor. Using multi-chip module package technology, the ŞµMMIT XT integrates the ŞµMMIT with internal memory, a memory management unit, and bus transceivers.

Operating either autonomously or with a tightly coupled host, the ŞµMMIT XT will solve a wide range of MIL-STD-1553 interface problems. A powerful RISC processing unit provides automatic message handling, message status, general status, and interrupt information. The register-based interface architecture provides many programmable functions, as well as, extensive information pertinent to device maintenance. In either of the three operating modes, the ŞµMMIT XT can access up to 32K x 16 of internal memory.

#### Memory Organization Control

Figure 1 is a block diagram of the ŞµMMIT XT, operating in 8 bit mode, interfacing with the UT69RH051 Microcontroller (hereinafter referred to as UT69RH051). The UT69RH051 has access to the ŞµMMIT XT's internal SRAM and registers, along with up to 64K x 8 of external PROM. Figure 1 also shows that the ŞµMMIT XT has the ability to auto-initialize; however, the PROM used for auto-initialization can be eliminated and the UT69RH051 can be used to initialize the ŞµMMIT XT. The choice is up to the designer.

Two software generated chip selects allow the UT69RH051 to select where it will read and write from. The UT69RH051's ALE signal is used to latch the address into both an external register and the ŞµMMIT XT's internal latches. The external register stores part of the 16 bit address used to access the PROM. Figures 2 and 3 show various memory access scenarios.

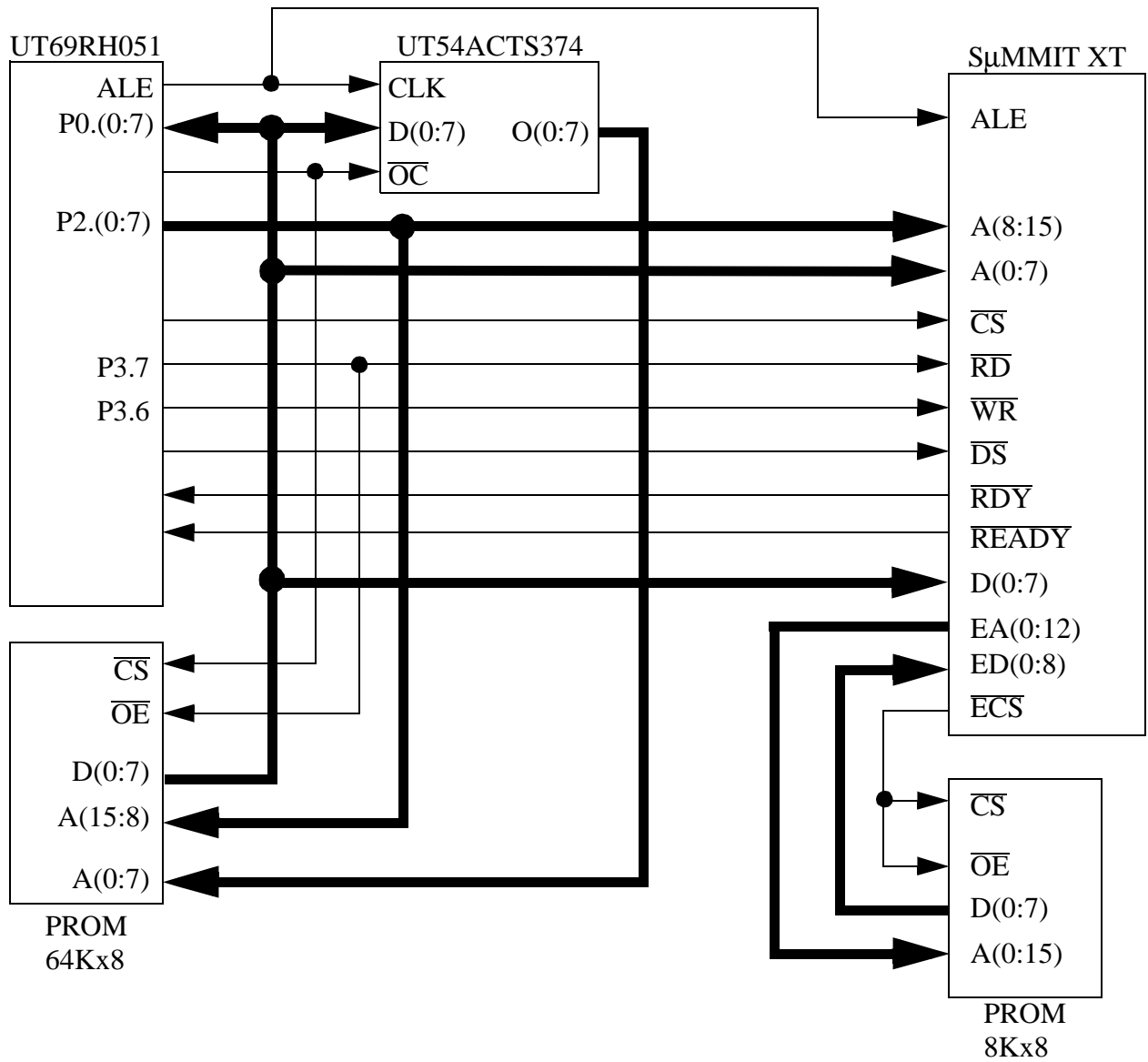


Figure 1: SμMMIT XT to UT69RH051 Microcontroller Interface Block Diagram

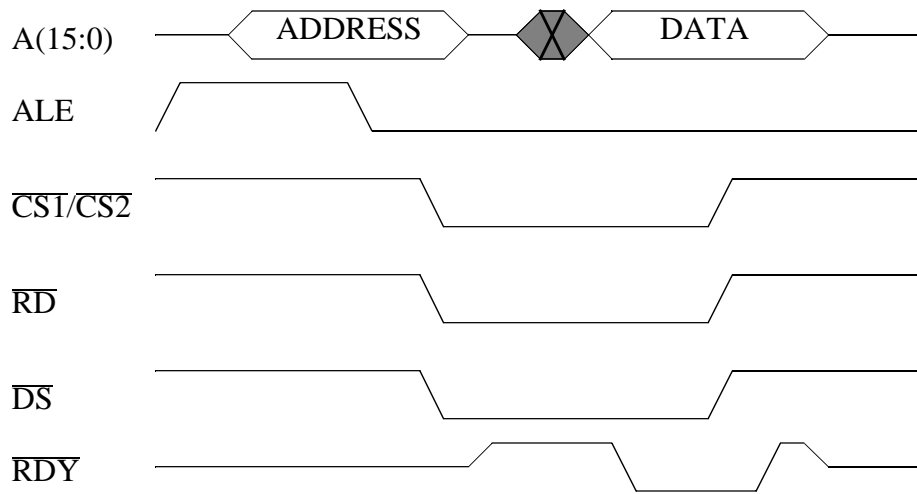


Figure 2. Multiplexed Memory, PROM and Register Read (8-Bit)

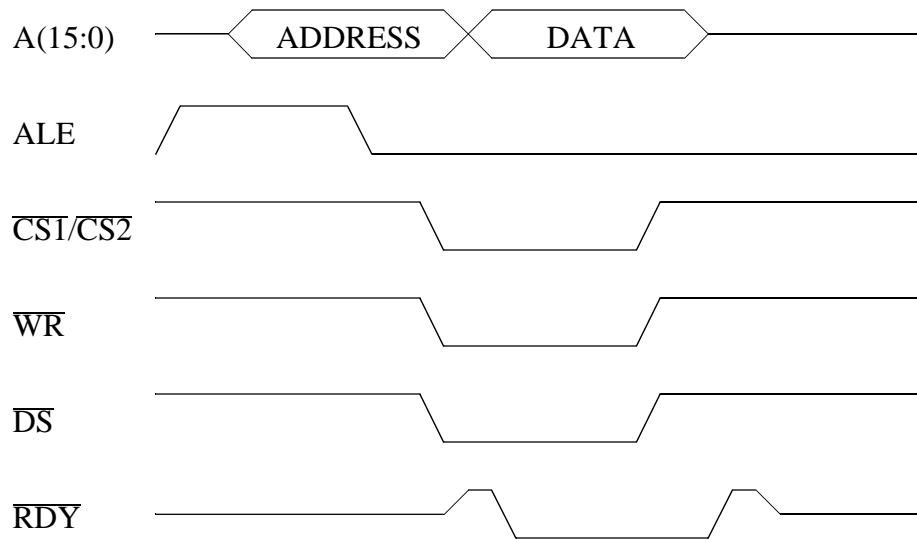


Figure 3. Multiplexed Memory and Register Write (8-Bit)