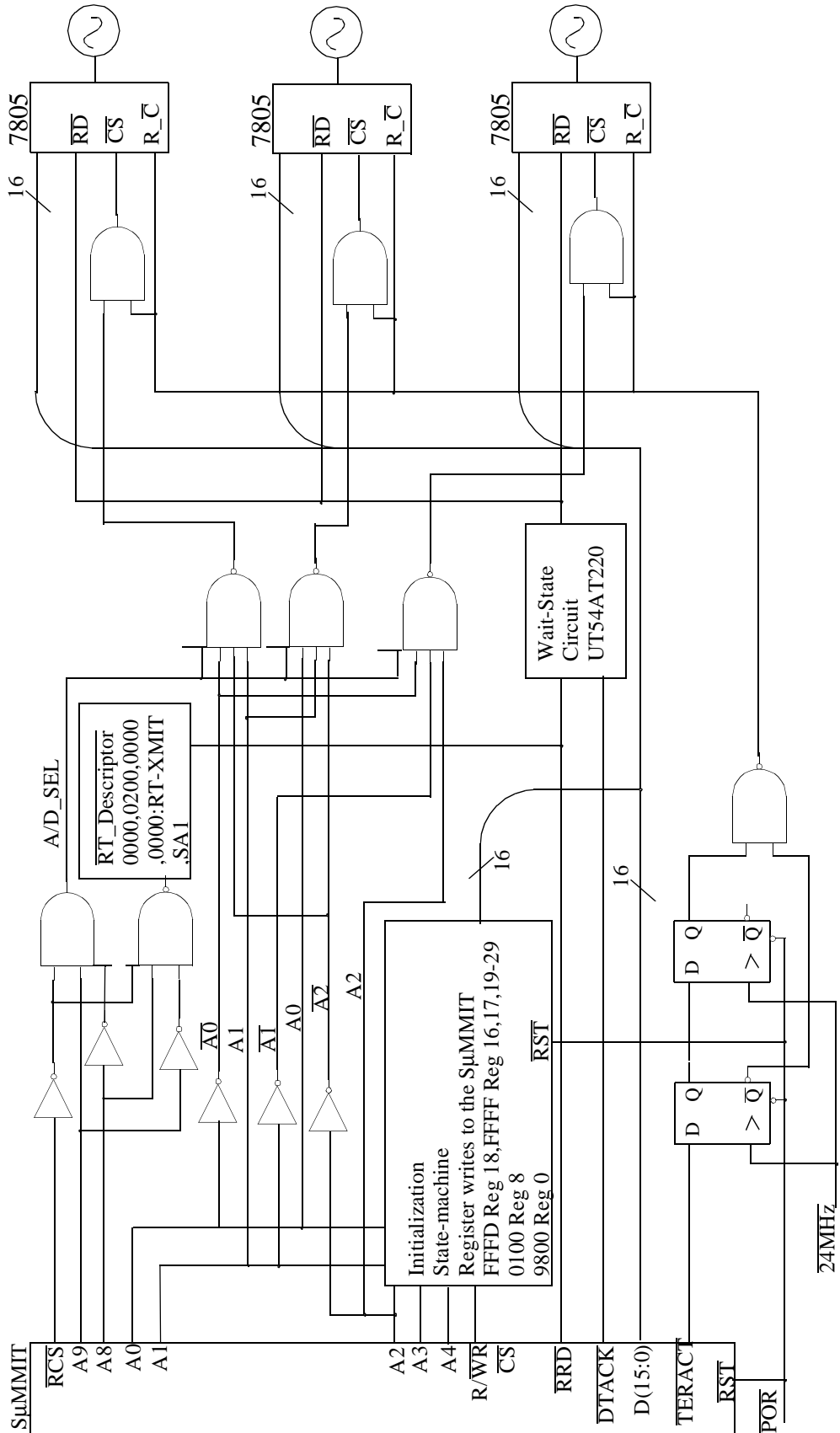


SμMMIT-to-7805 I/F



UTMC APPLICATION NOTE

S μ MMITTM LX to 7805 Interface

Basic Operation

For this application, the S μ MMIT LX interfaces to a PAL or equivalent logic device(s). The system does not allocate any memory for 1553 message storage. Instead, all data associated with 1553 message processing is retrieved from or stored into the PAL. The S μ MMIT LX will respond to a S/A 1 Transmit command (3 Data words) with the values read from the three 7805 A/D converters (mapped starting at address 0200h). All other S/A's and Mode-Codes are illegalized during the initialization sequence. Since the S μ MMIT LX requires four "housekeeping" words for each message transaction, usually stored in RAM, the PAL needs to accommodate the S μ MMIT LX "burst" DMA reads of four words after reception of the validated transmit command word. With ping-pong and broadcast operation disabled, only two of the four words (i.e., Control Word and Data Pointer A) are actually required. The Control Word and Data Pointer A are read first and second, respectively, in the DMA burst. The last two words are "don't care". At the end of message processing, the S μ MMIT writes/updates the Control Word and Data Pointer A. In this application the PAL discards/ignores any write information. To support message processing, the S μ MMIT reads or writes data words approximately every 20 μ S. For this application, the Bus Controller sends a Transmit 3 DW command every 100ms. The S μ MMIT Reference Manual and S μ MMIT Family Product Handbook contains additional timing diagrams and information on memory access.

Initialization and Mode of Operation

The PAL configures the S μ MMIT LX for operation by writing to the S μ MMIT LX's internal registers after master reset. For this very basic application, the PAL writes the following data into the S μ MMIT LX's Registers for setup and operation:

Data(hex)	Register	
FFFD	18	Legalize S/A#1.
FFFF	16-17	Illegalize all Receive S/A's.
FFFF	19-29	Illegalize all Mode Codes and Broadcast commands*.
0100	8	RT descriptor space pointer.
9800	0	Start the S μ MMIT, enable channels A and B.

*Note: Broadcast Transmit registers 22 and 23 are don't care (are automatically illegalized on reset).

Lock the S μ MMIT LX's mode of operation and remote terminal address on the rising edge of master reset by grounding the $\overline{\text{LOCK}}$ input. The S μ MMIT LX latches RTA(4:0), RTPTY and MSEL(1:0) on the rising edge of master reset. Select remote terminal operation by grounding MSEL(1) and tying MSEL(0) to five volts. Connect the A/ $\overline{\text{B}}$ input to ground for MIL-STD-1553B operation. The PAL can begin accessing the S μ MMIT 4.5 μ S after the rising edge of master reset. In order to minimize circuitry overhead, the RT descriptor is decoded with an address value of X1XX qualified with $\overline{\text{RCS}}$ and X2XX. The PAL responds back to the S μ MMIT LX with the following values (in sequence).

<u>Data(hex)</u>	<u>Read #</u>	
0000	1	S/A#1 Control Word
0200	2	Data Pointer A (Corresponds to A/D #1)
0000	3	Data Pointer B (Don't care).
0000	4	Broadcast Data Pointer (Don't care).

The PAL counts the \overline{RRD} pulses and places either 0000 or 0200₁₆ onto the data bus based on which read the S μ MMIT LX is executing. Once the S μ MMIT LX has completed all four read operations, it will place the address 0200₁₆ onto the address lines and perform three consecutive read operations (assuming that a Transmit 3 DW command was received) beginning at address 0202₁₆ (A/D#1), 0203₁₆ (A/D#2), 0204₁₆ (A/D#3). Since the A/D converters require approximately 8 μ S to acquire and lock-in the analog sample, \overline{TERACT} is used to detect the validated command and issue a single R_C pulse to all three A/D's.

Diagnostics

The S μ MMIT LX supports a comprehensive built-in test; either the bus controller or the PAL initiates built-in test. The bus controller initiates the built-in test via a mode code; the entire test sequence is automatic. The PAL could initiate a built-in test by using the following sequence: master Reset, wait 4.5 μ S, perform a Control Register write 4000₁₆, wait 1 μ S for self-test to complete, read BIT Word register. A Control Register write (i.e., 2000₁₆) invoking a software reset can replace the master reset.