

## UTMC Application Note

---

### S $\mu$ MMIT E & LXE/DXE JTAG Testability for the SJ02 Die

JTAG Instructions:

JTAG defines seven (7) public instructions as follows:

<b>Instruction</b>	<b>Status</b>	<b>UTMC Code msb..lsb</b>	<b>S<math>\mu</math>MMIT Status</b>
BYPASS	Mandatory	1111 (required all 1's)	Implemented
SAMPLE/PRELOAD	Mandatory	0010	Implemented
EXTEST	Mandatory	0000 (required all 0's)	Implemented
INTEST	Optional	0001	Implemented
RUNBIST	Optional	0111	Non-Compliant
IDCODE	Optional	0100 (reset instruction)	Implemented
USERCODE	Optional	Not Implemented	N/A

UTMC defines four (4) private instructions as follows:

<b>Instruction</b>	<b>Status</b>	<b>UTMC Code msb..lsb</b>	<b>S<math>\mu</math>MMIT Status</b>
GL-TRISTATE	Optional	0011	Implemented
INTERNAL-SCAN	Optional	0101	Used for RUNBIST
PRIVATE	Optional	0110	Not Implemented
USER-SELECTABLE	Optional	1000 -> 1110	Not Implemented

All JTAG operations are determined by the instruction residing in the JTAG instruction register. Instructions are entered into the instruction register by moving through the TAP controller state table with TCK and TMS. Once the SHIFT-IR state is reached, instruction bits are shifted into the TDI. Instructions are shifted LSB to MSB. The last instruction bit is entered when moving from the SHIFT-IR state to the EXIT1-IR state.

Setting the TAP Controller to the TEST-LOGIC-RESET state:

With TCK, TMS, TDI, at logic "1", pulse TRS active low for Xns, or, with TDI, TRS, TMS, at logic "1", clock TCK for 5 rising edges. The TAP controller will now be in the TEST-LOGIC-RESET state, and the IDCODE instruction is forced into the instruction register.

## JTAG Operation of the SμMMIT

JTAG signals:

Inputs: TCK - Test Clock  
TMS - Test Mode Select  
TDI - Test Data Input  
TRS - Test Reset, optional

Output: TDO - Test Data Output

JTAG signal rules:

- TMS is sampled on the rising edge of TCK.
- Change TMS on the falling edge of TCK.
- TDI is sampled on the rising edge of TCK.
- Change TDI on the falling edge of TCK.
- TDO changes on the falling edge of TCK.  
(TDO may cross the rising edge of the TCK clock boundary as TCK  $f_{MAX}$  increases)
- TMS should be a logic “1” while TRS changes from logic “0” to logic “1”.
- TDO is only ACTIVE when in either SHIFT-IR or SHIFT-DR TAP controller states. For SHIFT-IR, the instruction register is selected to drive TDO. For SHIFT-DR, the test data register is selected to drive TDO.

JTAG elements:

TAP - Test Access Port, includes the JTAG buffers plus drive for global JTAG signals.  
JM - JTAG Macro, contains the TAP controller, and the instruction register (IR).  
ENREG - Enable Register, holds the scan chain elements for the tri-state control.  
BSR - Boundary Scan Register, formed by the abutment of I/O cells.

JTAG TAP controller:

The TAP controller is a synchronous, finite, state machine that responds to changes in TCK and TMS.

The state of the TAP controller determines the state of the input, output, tri-state, and bi-directional buffers, as-well-as the function of TDI and TDO.

For “normal” chip operation, the user should always be in the TEST-LOGIC-RESET state. See the JTAG reset section for methods of selecting this TAP controller state. While the user is “IN” any other state, the instruction controls the state of the I/O buffers.

### **Instruction operation:**

- See the  $\mu$ MMIT Boundary Scan Register (BSR) order to determine the proper positioning of I/O cells, and the proper number of TCK's needed to shift in/out the BSR contents.
- Always return to the TEST-LOGIC-RESET state when JTAG operation completes.

### **IDCODE** (UTMC calls ID-SCAN)

#### Objective:

The objective of IDCODE is to shift out of TDO, the  $\mu$ MMIT's IDCODE.

#### Method:

From the TEST-LOGIC-RESET state (IDCODE is the default instruction), move to the SHIFT-DR state and apply 33 TCK clock cycles. The first bit out of TDO will always be a logic "1" followed by the 32 bit IDCODE. The IDCODE instruction can also be entered into the instruction register by moving to the SHIFT-IR state and applying the IDCODE instruction to TDI. Then move to the SHIFT-DR state and apply 33 TCK clock cycles.

The state of I/O buffers when IDCODE is loaded into the IR:

Normal operation.

### **SAMPLE/PRELOAD**

#### Objective:

The objective of SAMPLE/PRELOAD is to sample the component inputs or preload the component output data registers.

#### Method:

From the TEST-LOGIC-RESET state, move to the SHIFT-IR state and apply the SAMPLE/PRELOAD instruction to TDI. Then move to the CAPTURE-DR state. At this time, the inputs are captured and can be shifted out through TDO if the SHIFT-DR state is entered. As captured inputs are shifted out of TDO, the component outputs can be preloaded by applying proper data to TDI. The actual preload occurs when the UPDATE-DR state is entered. Preloading is used before the EXTEST instruction is applied.

The state of the I/O buffers when SAMPLE/PRELOAD is loaded into the IR:

Normal operation.

## RUNBIST

Objective:

The objective of the RUNBIST is to trigger the execution of a self-contained self-test.

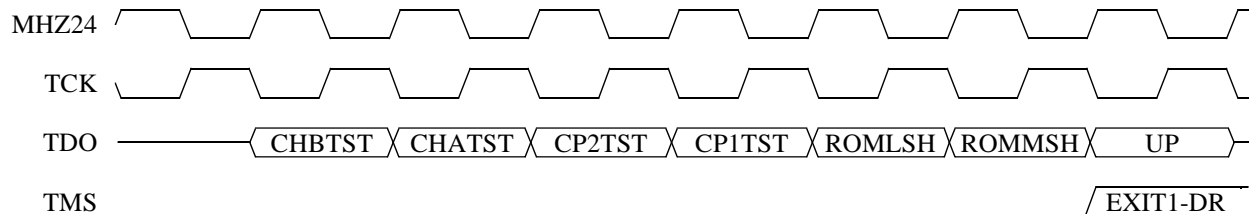
Method:

The RUNBIST Sequence of Events -

1. Follow the SAMPLE/PRELOAD instructions to shift in the desired values to be applied to the inputs and outputs for duration of the RUNBIST instruction.
2. Free running system clock (MHZ24).
3. Move to the SHIFT-IR state and apply the RUNBIST instruction to TDI.
4. Move to the RUN-TEST/IDLE state, self-test starts.
5. Run the system clock for 16,000 cycles.
6. Stop the system clock.
7. Move to the SHIFT-DR state and apply 7 TCK falling edges to shift the self-test results out through TDO. The order of the test bits is as follows: CHBTST, CHATST, CP2TST, CP1TST, ROMLSH, ROMMSH, UP.

Notes: Event 4 and 7 are S $\mu$ MMIT variations from the JTAG rules, and are used as follows:

4. The self-test begins operation at the UPDATE-IR state when the RUNBIST instruction becomes active, NOT when the RUN-TEST/IDLE state is reached.
7. Move to the SHIFT-IR state and apply the INTERNAL-SCAN instruction to TDI. Then move to the SHIFT-DR state and apply TCK and MHZ24 as shown below.



The state of the I/O buffers when RUNBIST is loaded into the IR:

Inputs are blocked from the on-chip logic and outputs are driven with the preloaded values for the duration of the RUNBIST.

## **EXTEST**

### Objective:

The objective of EXTEST is to drive the component outputs, and to capture the component inputs.

### Method:

From the TEST-LOGIC-RESET state, move to the SHIFT-IR state and apply the EXTEST instruction to TDI. Then move to the UPDATE-IR state, at this time the data preloaded into the output data registers are driven to the outputs.

To capture new inputs and drive new outputs, move to the CAPTURE-DR state, at this time the inputs are captured and can be shifted out through TDO if the SHIFT-DR state is entered. As captured inputs are shifted out of TDO, component outputs can be preloaded by applying proper data to TDI. Then move to the UPDATE-DR state, at the next TCK falling edge the outputs will change to the preloaded values. Repeat the above sequences to continue sampling inputs and driving outputs.

The state of the I/O buffers when EXTEST is loaded into the IR:

Inputs operate as normal, outputs are driven with preloaded values, normal system outputs are inhibited from exiting the component as long as EXTEST resides in the instruction register.

## **BYPASS**

### Objective:

The objective of BYPASS is to form a connection between TDI and TDO.

### Method:

From the TEST-LOGIC-RESET state, move to the SHIFT-IR state and apply the BYPASS instruction to TDI. Then move to the SHIFT-DR state, TDI will now be connected to TDO. The first bit out of TDO will always be a logic "0" followed by bits applied to TDI.

The state of I/O buffers when BYPASS is loaded into the IR:

Normal operation.

## **INTEST**

### Objective:

The objective of INTEST is to perform slow-speed testing of the on-chip logic with each test pattern, with the response being shifted through the boundary scan register (BSR).

### Method:

The INTEST Sequence of Events -

1. Follow the SAMPLE/PRELOAD instructions to shift in the desired values to be applied to the inputs and outputs for the first INTEST test vector.
2. Stop the system clock (MHZ24).
3. From the UPDATE-DR state, move to the SHIFT-IR state and apply the INTEST instruction to TDI. Then move to the UPDATE-IR state. At this time, the data preloaded into the output data registers are driven to the outputs.
4. Return to the RUN-TEST/IDLE state.
5. Pulse the system clock once. (see JTAG figure 7-8)
6. Move to the SHIFT-DR state to shift the next test vector being applied to the inputs and outputs through the TDI.
7. If the test is NOT complete, goto step #4.

The state of the I/O buffers when INTEST is loaded into the IR:

Inputs are blocked from on-chip logic and outputs are driven with the preloaded values of each test vector.

## **GL-TRISTATE**

### Objective:

The objective of GL-TRISTATE is to set the tri-state and bi-directional buffers to the floating output state without having to shift-in the values for the enables via the BSR. This instruction is provided as a convenience to the user for I/O enable control. It also facilitates testing for DC input levels and  $Q_{IDD}$ .

### Method:

Move to the SHIFT-IR state and apply the GL-TRISTATE instruction to TDI. Then move to the UPDATE-IR state. At this time, all tri-state and bi-directional buffers are floated.

The state of the I/O buffers when the GL-TRISTATE is loaded into the IR:

All tri-state and bidirectional buffers are set to the floating state of operation.

## SμMMIT JTAG Boundary Scan Register (BSR) Order

It takes 123 TCK's to shift in/out the entire BSR contents.

There are 33 inputs and 12 outputs that are not bonded out in the PGA85/FP84 packages, but MUST be considered when shifting data in/out of the BSR.

Position #1 is the first bit which would appear at TDO if the user was shifting out the contents of the BSR.

MHZ24 is a ICNCLK input buffer, and can only be sampled. The input mode CAN NOT be disabled or altered by JTAG control.

**Table 1: SμMMIT JTAG BSR Order**

Position	Name	BSR Type
1	DMARB Enable	ENREG
2	ROMENB Enable	ENREG
3	YF_INTB Enable	ENREG
4	MSGINTB Enable	ENREG
5	ADDRESS Enable	ENREG
6	Data Enable	ENREG
7	DUMMY (PC0)	Output
8	DUMMY (PC1)	Output
9	MRSTB	Input
10	DUMMY (PC2)	Output
11	MDSEL0	Input
12	DUMMY (PC3)	Output
13	MDSEL1	Input
14	DUMMY (PC4)	Output
15	DUMMY (PC5)	Output
16	DUMMY (PC6)	Output
17	ABBSTD	Input
18	LOCKB	Input

**Table 1: S $\mu$ MMIT JTAG BSR Order**

<b>Position</b>	<b>Name</b>	<b>BSR Type</b>
19	RTPTY	Input
20	DUMMY (PC7)	Output
21	RTA0	Input
22	DUMMY (PC8)	Output
23	RTA1	Input
24	DUMMY (PC9)	Output
25	DUMMY (PC10)	Output
26	RTA2	Input
27	DUMMY (PC11)	Output
28	RTA3	Input
29	RTA4	Input
30	SSYSFB	Input
31	READYB	Output
32	TERACB	Output
33	RB	Input
34	RBB	Input
35	TB	Output
36	TBB	Output
37	TMRONBB	Output
38	RA	Input
39	RAB	Input
40	TA	Output
41	TAB	Output
42	TMRONAB	Output
43	D0	Bi-Direct
44	D1	Bi-Direct
45	D2	Bi-Direct

**Table 1: S $\mu$ MMIT JTAG BSR Order**

<b>Position</b>	<b>Name</b>	<b>BSR Type</b>
46	D3	Bi-Direct
47	D4	Bi-Direct
48	D5	Bi-Direct
49	D6	Bi-Direct
50	D7	Bi-Direct
51	DUMMY (EXISEL)	Input
52	D8	Bi-Direct
53	DUMMY (EXI0)	Input
54	D9	Bi-Direct
55	DUMMY (EXI1)	Input
56	D10	Bi-Direct
57	DUMMY (EXI2)	Input
58	DUMMY (EXI3)	Input
59	D11	Bi-Direct
60	D12	Bi-Direct
61	D13	Bi-Direct
62	DUMMY (EXI4)	Input
63	D14	Bi-Direct
64	DUMMY (EXI5)	Input
65	D15	Bi-Direct
66	DUMMY (EXI6)	Input
67	DTACKB	Input
68	TCLK	Input
69	DUMMY (EXI7)	Input
70	RCSB	Tri-State
71	RRDB	Tri-State
72	RWRB	Tri-State

**Table 1: S $\mu$ MMIT JTAG BSR Order**

<b>Position</b>	<b>Name</b>	<b>BSR Type</b>
73	DUMMY (EXI8)	Input
74	A0	Bi-Direct
75	DUMMY (EXI9)	Input
76	A1	Bi-Direct
77	DUMMY (EXI10)	Input
78	A2	Bi-Direct
79	DUMMY (EXI11)	Input
80	A3	Bi-Direct
81	A4	Bi-Direct
82	DUMMY (EXI12)	Input
83	A5	Tri-State
84	DUMMY (EXI13)	Input
85	A6	Tri-State
86	DUMMY (EXI14)	Input
87	DUMMY (EXI15)	Input
88	MHZ24	Input
89	DUMMY (EXI16)	Input
90	A7	Tri-State
91	DUMMY (EXI17)	Input
92	A8	Tri-State
93	A9	Tri-State
94	DUMMY (EXI18)	Input
95	A10	Tri-State
96	DUMMY (EXI19)	Input
97	A11	Tri-State
98	DUMMY (EXI20)	Input
99	A12	Tri-State

**Table 1: S $\mu$ MMIT JTAG BSR Order**

<b>Position</b>	<b>Name</b>	<b>BSR Type</b>
100	DUMMY (EXI21)	Input
101	A13	Tri-State
102	DUMMY (EXI22)	Input
103	A14	Tri-State
104	DUMMY (EXI23)	Input
105	A15	Tri-State
106	RDWRB	Input
107	CSB	Input
108	ROMENB	Tri-State
109	DUMMY (EXI24)	Input
110	DUMMY (EXI25)	Input
111	DUMMY (EXI26)	Input
112	DUMMY (EXI27)	Input
113	AUTOENB	Input
114	DUMMY (EXI28)	Input
115	YFINTB	Tri-State
116	DUMMY (EXI29)	Input
117	MSGINTB	Tri-State
118	DMACKB	Tri-State
119	DUMMY (EXI30)	Input
120	DMAGB	Input
121	DUMMY (EXI31)	Input
122	DMARB	Tri-State
123	DUMMY (PCK)	Output