

## SmMMIT™ XTE and RTE RT-Mode Self-Test Anomaly

Table 1: Cross Reference of Affected Products

Product Name:	SMD #:	Device Type:	Internal PIC Number:
UT69151XTE	5962-94758	07	MM019B, MM020B, MM021B,
	5962-94758	08	MM019C, MM020C, MM021C,
	5962-94758	09	MM019D, MM020D, MM021D
UT69151RTE	5962-98587	01	MM022B

### 1.0 Overview

This product errata is provided by Aeroflex UTMC to describe the SμMMIT™-XTE and SμMMIT™-RTE Remote Terminal Mode operation with regard to the internal Self-Test function. Any use of the Self-Test for these products should adhere to the following guidelines. Affected operating Modes for the SμMMIT™-XTE and SμMMIT™-RTE are Remote Terminal (Mode Select 0 = logic value one, and Mode Select 1 = logic level zero) and concurrent Remote Terminal/Monitor for SμMMIT™-XTE only (Mode select 0 = logic value one, and Mode Select 1 = logic level one). Throughout this document  $\overline{\text{READY}}$  is referred to as an output pin. The SμMMIT™-XTE and SμMMIT™-RTE Status Register (Register 1) READY (bit 1) function is not altered from the description in the SuMMIT Family Product Handbook and still provides an inverted reflection of the  $\overline{\text{READY}}$  output pin.

There are two of Self-Test functions performed by the SμMMIT™-XTE and SμMMIT™-RTE devices:

- 1) Host initiated;
- 2) Mode Code 3 initiated (MC3).

The two Self-Test functions are distinguished by the operations performed. The MC3 Self-Test will take approximately 1mS to complete, will perform a protocol section self-test and will not perform a memory test. The Host initiated Self-Test will perform both a protocol and memory test. After execution of the Host initiated Built-In Test (BIT), all memory descriptor and pointer values must be re-initialized.

#### 1.1 Host Initiated BIT

The Host initiated Self-Test function is effected through the local processor interface by writing a value of 4000 hex to the SμMMIT™ Control Register (Register 0). When a Host initiated Self-Test is invoked, the SμMMIT™-XTE and SμMMIT™-RTE will perform a verification of the protocol and memory sections of the device. If the Self-Test results are without errors, the device will set the Self-Test associated bits ( 8, 9, 10, 11 and 12) in Register 6 to a logic value of zero. If an error is encountered during the Self-Test, the device will set the Terminal Flag (bit 0) in Register 9 to a logic-level one, the BIT fail (bit 12) and the associated cause bit(s) in Register 6 ( bits 8, 9, 10, 11) to a logic value of one. For the period of time the Self-Test is being performed, the external  $\overline{\text{READY}}$  and BIST outputs are set to a logic level one, and logic level zero state respectively. The  $\overline{\text{READY}}$  output is set to a logic-level one during the internal protocol test, for a period of approximately 1mS. The BIST output is set to a logic-level zero during the internal memory test, for a period of approximately 70mS for the SμMMIT™-XTE and 18mS for the SμMMIT™-RTE.

#### 1.2 Mode Code Initiated BIT

The Mode Code Self-Test function is invoked through the 1553 bus Mode Code 3 (MC3). When a MC3 initiated Self-Test is invoked, the SμMMIT™-XTE and SμMMIT™-RTE will perform a verification of the Protocol section of the device. If the Self-Test results are without error, the device will set the Self-Test associated bits ( 8, 9, 10, 11 and 12) in Register 6 to a logic value of zero. If an error is encountered during the Self-Test, the device will set the Terminal Flag (bit 0) in Register 9 to a logic-level one, the BIT fail (bit 12) and the associated cause bit(s) in Register 6 ( bits 10, 11) to a logic value of one. During the Self-Test operation, the external  $\overline{\text{READY}}$  output is set to an inactive state (logic level one state) for a period of approximately 1mS.

A pairing of the Initiate Self-Test (Mode Code 3) and Transmit BIT Word (Mode Code 19) is a typical system process that initiates a Self-Test (MC3) and reports the status/result (MC 19) of the Self-Test.

## 2.0 BIST Output Pin Discussion

### 2.1 Current Operation

The BIST output pin (FP 114, PGA D10) no longer tracks the internal memory test operation during the Host initiated BIT for the listed devices in Table 1. After the S $\mu$ MMIT<sup>TM</sup>-XTE and S $\mu$ MMIT<sup>TM</sup>-RTE devices are reset, the BIST output pin will remain in a logic-level zero state. When a Host initiated Self-Test is invoked, the S $\mu$ MMIT<sup>TM</sup>-XTE and S $\mu$ MMIT<sup>TM</sup>-RTE will perform a verification of the Protocol and Memory sections of the device. The READY output will go to a logic-level one state and remain inactive for the entire period of the internal protocol, and internal memory test (approximately 70mS for the XTE and 18mS for the RTE).

### 2.2 Work-around

The Host should now monitor only the READY output pin (FP 110, PGA D9) for the on-going status of the Host invoked Self-Test. The READY output pin will accurately track the Self-Test period for the MC3, or Host initiated in both the S $\mu$ MMIT<sup>TM</sup>-XTE and S $\mu$ MMIT<sup>TM</sup>-RTE.

## 3.0 Mode Code 3 Discussion

### 3.1 Current Operation

After completion of the internal Self-Test without an error indication, (as instigated by a standard 1553 Self Test Mode Code 3 command) the S $\mu$ MMIT<sup>TM</sup>-XTE and S $\mu$ MMIT<sup>TM</sup>-RTE will respond with a proper Status Word Response (Clear Response). However, if a follow-up command of Transmit BIT Word Mode Code (Mode Code 19) is received by the listed devices in Table 1, the S $\mu$ MMIT<sup>TM</sup>-XTE and S $\mu$ MMIT<sup>TM</sup>-RTE will respond with a proper Status Word Response (Clear Response) but the associated Data Word will contain the hexadecimal value of 1023 indicating a BIT fail occurred in response to the previously executed Mode Code 3. The expected response to a Mode Code 19 when a true Self-Test error occurred is a Status Word Response with the Terminal Flag bit set (bit time 19) along with the BIT fail bit and corresponding information bits in the associated Data Word.

### 3.2 Work-around

The Host can circumvent and correct the improper response by the S $\mu$ MMIT<sup>TM</sup>-XTE and S $\mu$ MMIT<sup>TM</sup>-RTE to MC19 by using the Sub-Address Accessed interrupt (enabled in Register 3, bit 10 and bit 6 of the MC3 Descriptor Control Word). Implementing this work-around is the best solution since it eliminates the need for a Bus Controller/System Mode Code 19 interpretation and produces a normal response to a Mode Code 3 and 19 command set. Since the Bus Controller will receive only correct status and data responses to MC3/MC19 commands, there is no impact, or notification required to the system user. The interrupt implementation allows a maximum Host time window for the Register 9 interrogation and Register 6 update. Properly implementing this work-around will create a correct response to a Mode Code 3 and subsequent MC19 command as indicated with a Clear Status Word response and the associated Data Word bits 0 through 12 set to a logic level zero when no Self-Test error has occurred. The MC3/MC19 response when a real Self-Test error occurs will also be corrected to accurately reflect the true failure condition (MC19 Status Word response with the Terminal Flag set) and only pertinent values set for Self-Test and System status bit in the MC19 Data Word. The timing and process for the Host Mode Code 3 intervention is as follows.

Once the Host receives the interrupt generated at the completion of the Mode Code 3 command, the Host should read the S $\mu$ MMIT<sup>TM</sup>-XTE and S $\mu$ MMIT<sup>TM</sup>-RTE Register 9 and verify the state of the Terminal Flag (bit 0). If the Terminal Flag (bit 0) is not set to a logic-level one in Register 9 after execution of the Mode Code 3 command, the BIT Register 6, bits 0 through 12 can be set to a logic level zero by the Host. Bits 13, 14, and 15 of Register 6 are valid regardless of the Terminal Flag state and can be evaluated by the Host for the associated RT status. The latency period for the Host's evaluation of Register 9 and update of Register 6 is 10 $\mu$ S or less. To clarify, the latency period of 10 $\mu$ S is from the MSG\_INT assertion of the related MC3

completion and the update/write to Register 6. The 10 $\mu$ S window will provide adequate time for the correction to complete assuming a MC19 Command was validated 4 $\mu$ S (1553 Command Gap minimum period) after the Mode Code 3 command.

### 3.3 Alternate Work-around

The implementation of this work-around will impact System-level users since the evaluation of the S $\mu$ MMIT<sup>TM</sup>-XTE and S $\mu$ MMIT<sup>TM</sup>-RTE response to the MC3/MC19 command set is performed at the 1553 Bus Controller level.

The Bus Controller/System can determine whether a true Self-Test error occurred with a previously executed MC3 through the evaluation of the Status Word response to the Transmit BIT Word Mode Code (MC19). If the Terminal Flag (bit time 19) is not set in the Mode Code 19 Status Word response, the Bus Controller must ignore the associated Data Word bit 0 through 12 values. Bits 13, 14, and 15 of the MC 19 Data Word are valid regardless of the Terminal Flag state, and can be evaluated by the Bus Controller for the associated RT status. If the Terminal Flag, bit time 19 is set (logic value of one) in the Mode Code 19 Status Word response, the Bus Controller can evaluate the associated Self-Test Data Word bits 8, 9, 10, 11 and 12 as well as bits 13, 14, and 15 of the MC 19 Data Word for failure clarification; all other Data Word bit values (bits 0 through 7) should be disregarded.