

UTMC Errata Sheet

UT69151 SμMMIT RTE Register Compliance

UTMC has identified the following deviation from intended functional performance for prototype and reduced high reliability versions of the UT69151 SμMMIT RTE (device code MM022A).

Background:

The UT69151 SμMMIT RTE contains a MIL-STD-1553 protocol handler, Memory Management Unit (MMU), 4K x 16 of SRAM, and transceivers. The MMU is responsible for managing host and protocol accesses to memory, along with host accesses to the protocol handler's internal registers. The protocol handler's internal registers contain status and configuration information. A recent evaluation of the UT69151 SμMMIT RTE internal memory and register architecture has identified an anomaly in the MMU's ability to process host read and write cycles while the protocol handler is processing a MIL-STD-1553 message.

If the host processor attempts either a memory or registers cycle while $\overline{\text{TERACT}}$ is low, the host cycle is corrupted. The SμMMIT RTE indicates that MIL-STD-1553 message processing has started by asserting $\overline{\text{TERACT}}$ (i.e., active low). $\overline{\text{TERACT}}$ remains low until MIL-STD-1553 message processing completes. For write cycles, no data is written into either the protocol handlers register or into the cycle specific address location. For read cycles, invalid data is presented to the host on the SμMMIT RTE's external data bus. The anomaly occurs in all modes of operation bus controller, remote terminal and monitor. Additionally, the anomaly is independent of device is configuration, i.e., multiplexed, non-multiplexed, 8-bit mode, 16-bit mode.

Figure 1. Corrupted Write Cycles

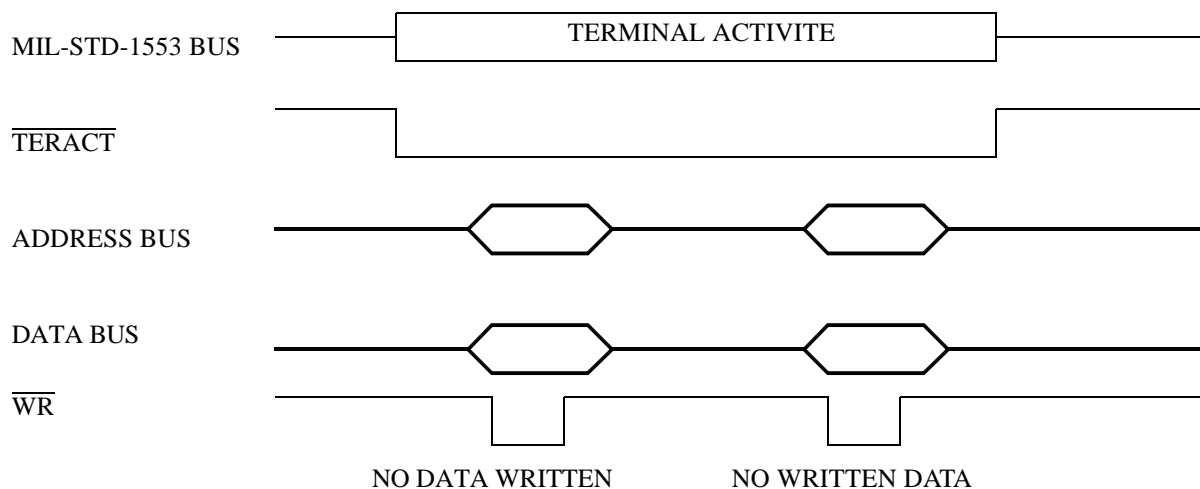


Figure 2. Corrupted Read Cycles

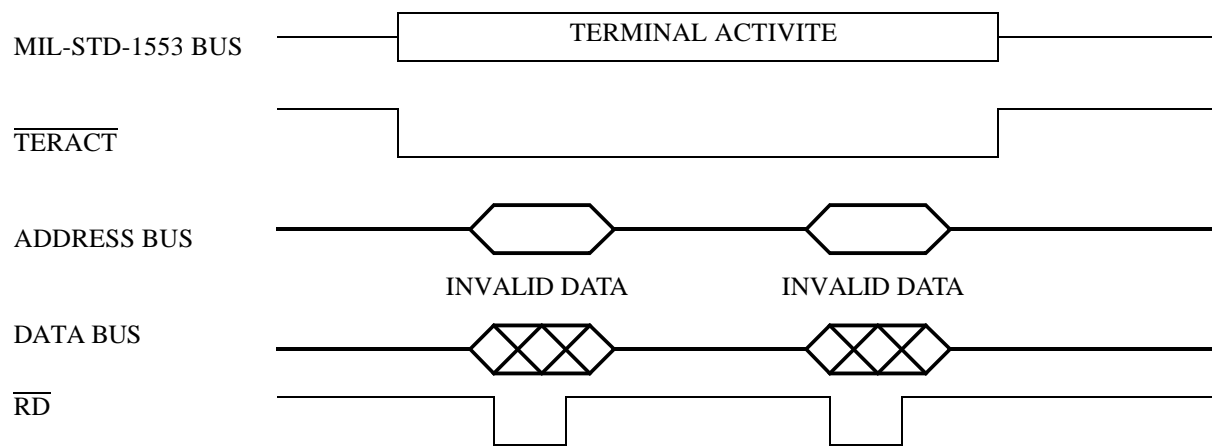


Figure 3. Valid Write Cycles

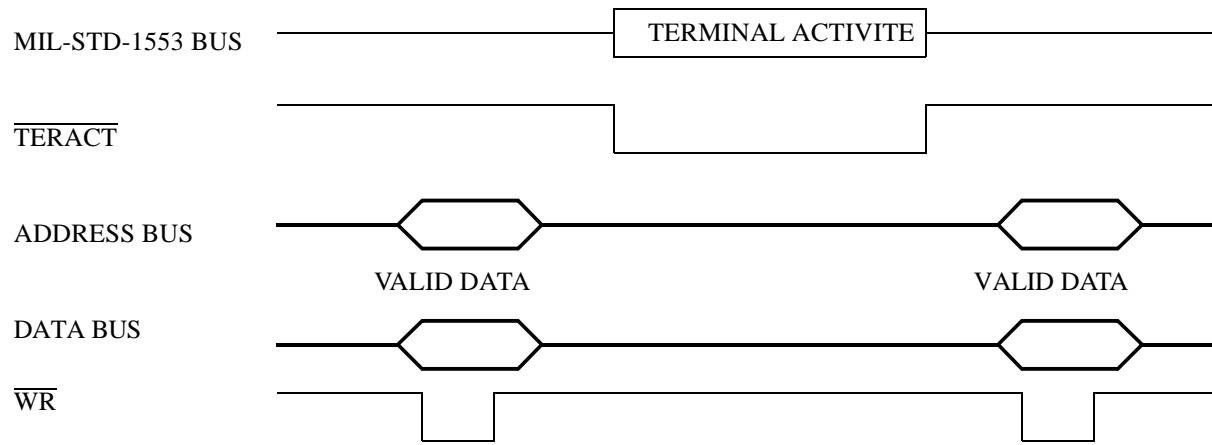
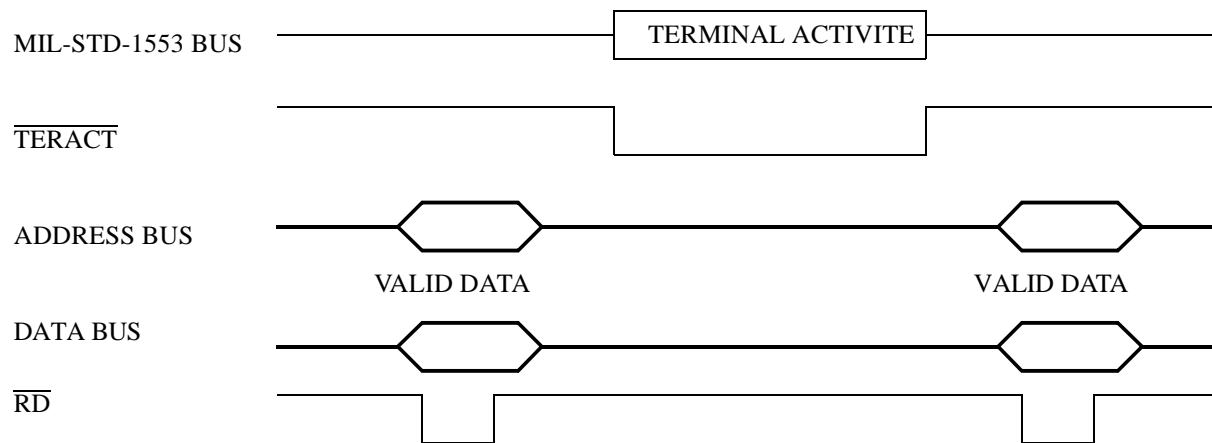


Figure 4. Valid Read Cycles



Work-Around:

The production revision of the UT69151 SμMMIT RTE (MM019B) will incorporate a circuit change to the MMU eliminating register and memory bus corruption during memory/register accesses occurring concurrently with MIL-STD-1553 message processing. Production versions of the UT69151 SμMMIT RTE, with the design fix, are scheduled for end 4Q98 deliveries. A system work-around is to eliminate memory or register accesses while the SμMMIT RTE is processing MIL-STD-1553 messages.