

Common Mode Considerations for the Aeroflex UTMC S μ MMITTM XTE Product Family

Table 1: Cross Reference of Applicable Products

Product Name:	SMD #	Device Type	Internal PIC Number:
S μ MMIT XTE (5V)	5962-94758	08	MM019
S μ MMIT XTE (12V)	5962-94758	09	MM020
S μ MMIT XTE (15V)	5962-94758	07	MM021

1.0 Overview

Aeroflex UTMC's analysis of the S μ MMIT XTE's in-system, functional operation has identified some important common mode related issues. These common mode issues are relevant for scenarios where the S μ MMIT XTE receives signals from a source that does not share power and ground planes with the S μ MMIT XTE. In a system where the ground of the source electronics lacks the necessary low inductance current path (less than 5nH) to the S μ MMIT XTE ground, read failures can occur. The typical failure mode exhibits itself in the form of bad data reads or incorrect memory read cycle termination.

Table 1, identifies all applicable S μ MMIT XTE product covered in this advisory. Previous versions of the S μ MMIT XTE are not at risk of the common mode failures discussed within this advisory because they are built with slower technology, and do not have the same number of simultaneous switching I/O.

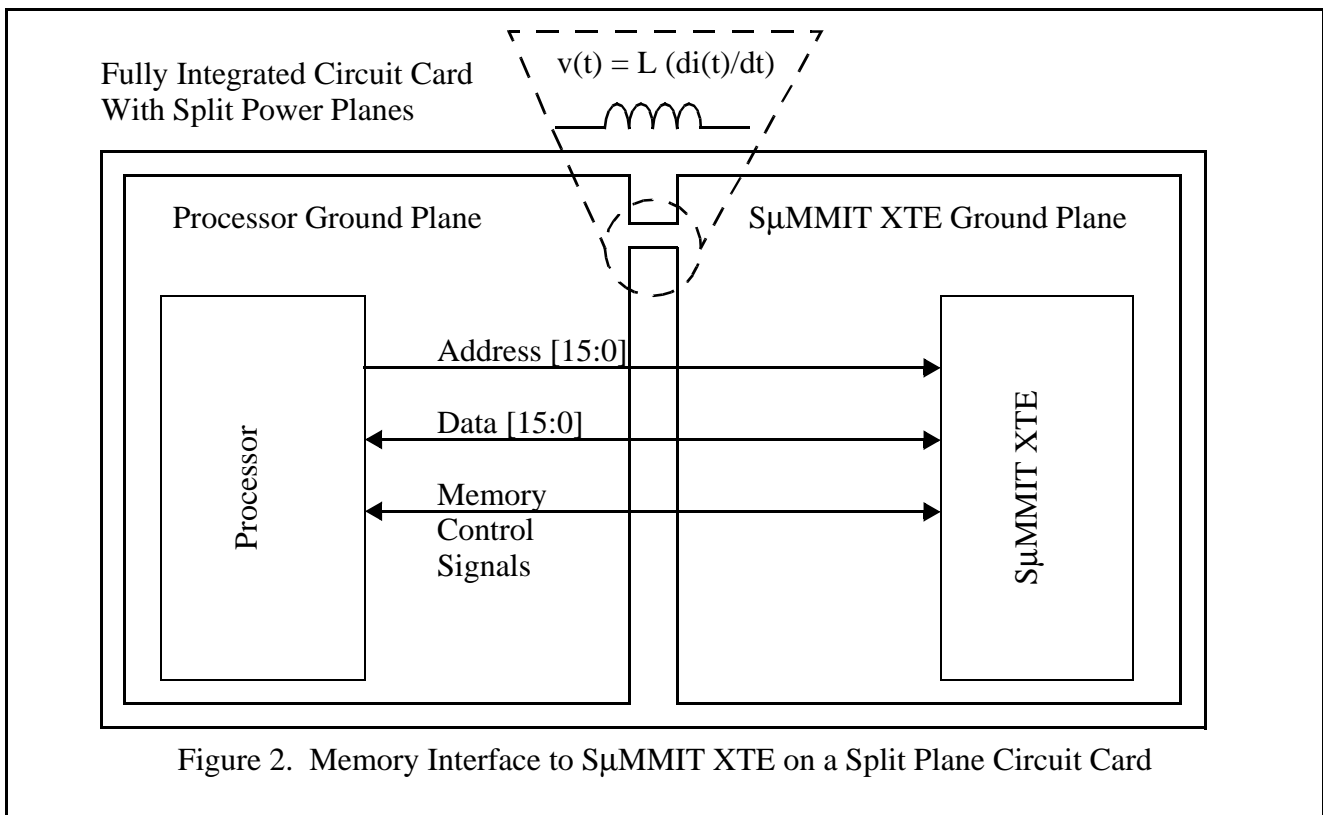
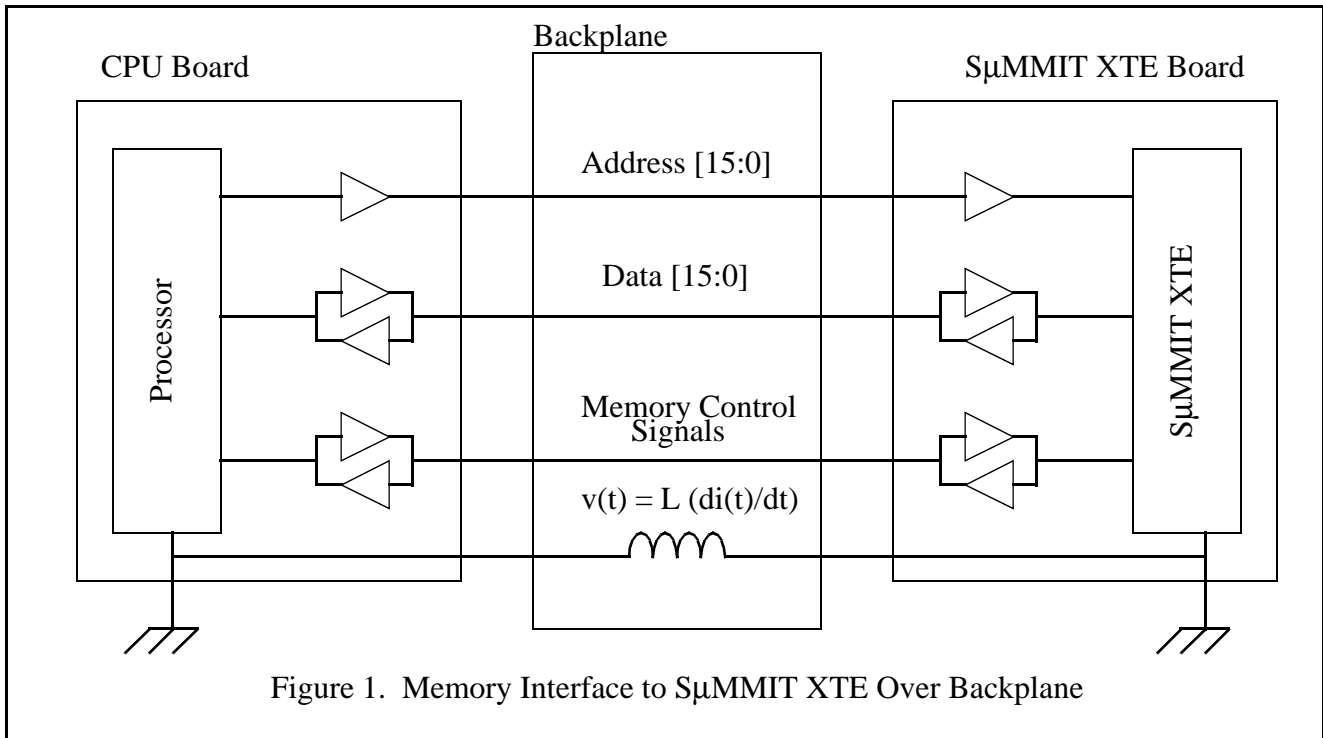
2.0 At Risk Systems

A system is at risk when the memory interface signals to the S μ MMIT XTE do not share a power and ground plane with the S μ MMIT XTE. The applicable memory interface signals include:

1. Address [15:0],
2. Data [15:0],
3. \overline{ALE} ,
4. \overline{RD} ,
5. \overline{CS} , and
6. \overline{DS}

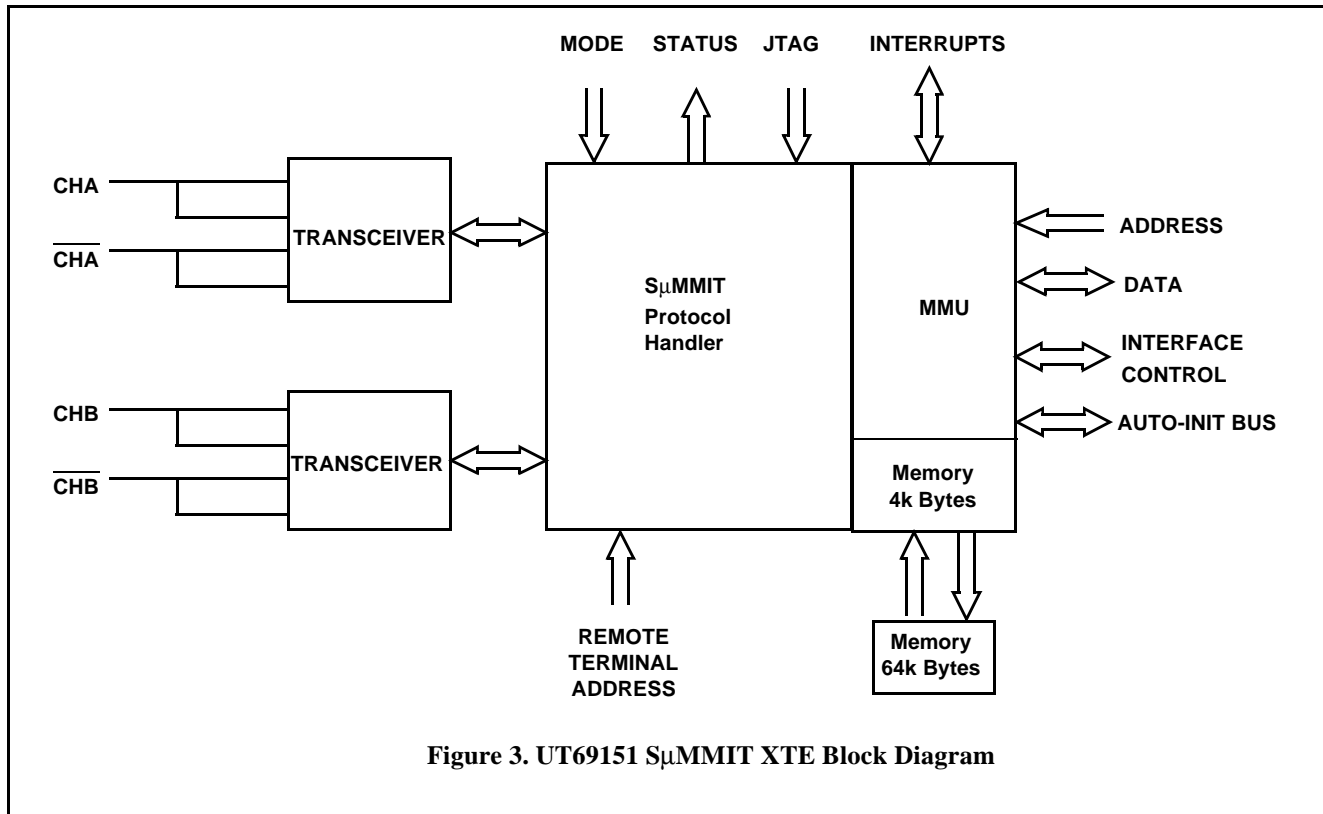
These memory interface signals must be common moded out in order to ensure proper functional operation of the S μ MMIT XTE particularly during memory reads. If any of these signals are electrically manipulated by a component, which does not share the power and ground planes with the S μ MMIT XTE, the system is at risk of common mode failures.

Some typical systems exhibiting failures include those where the memory reads across a backplane are initiated by a processor on a different module than the S μ MMIT XTE (Figure 1), and systems whose memory cycle activities are all contained on the same module, but the S μ MMIT XTE uses different power planes than the device performing memory accesses to the S μ MMIT XTE (Figure 2).



2.1 Failure Mechanism

The primary cause of read failures in the systems described in section 2.0 above occur because of the high inductive current path between the ground plane of the S μ MMIT XTE and the ground plane of the device performing a memory read. This inductive current path plays a major role during memory reads to the S μ MMIT XTE because of the large simultaneous switching current induced by the S μ MMIT XTE. The S μ MMIT XTEs identified in Table 1 of this document consist of a 4 die, multi-chip module architecture as shown by the functional block diagram in Figure 3 below.



During a memory read, the memory interface signals are directly interpreted by the Memory Management Unit (MMU) located in the S μ MMIT protocol die. The MMU determines whether the memory access is multiplexed or non-multiplexed, 8-bits or 16-bits in size, and whether the access is being made to the S μ MMIT Configuration Registers, the local 4kByte SRAM or the external 64kByte SRAM. As a result, a number of devices, and buffers can be simultaneously switched from an “OFF” or lower power state to an active high current state. An example would be reading a 16-bit word from the external 64kByte memory. Such a scenario causes the S μ MMIT protocol chip to activate 16 address buffers to the memory, bring the memory from an idle to an active operating state, allow the high speed external memory to drive data to the S μ MMIT, and enable the 16 data buffers from the S μ MMIT to the host. All of this simultaneous activity causes a large current surge into the ground plane via the S μ MMIT XTE.

Typically, a very good decoupling scheme will provide an efficient current return path from the V_{SS} pins to the V_{DD} pins on the S μ MMIT XTE. However, due to the parasitics of the chip capacitors (e.g. effective series resistance) the current path is not perfect, and the excess current must find an alternative return path through the system. Additionally, it is difficult to decouple a complex circuit for all relevant current frequencies, further affecting the amount of excess current that is not efficiently routed through the decoupling capacitor.

For systems described in section 2.0, the excess current flow on the S μ MMIT XTE’s power planes result in power and ground bounce that is not well matched by power and ground bounce at the device reading the S μ MMIT XTE. This is a direct result of the large impedance between power planes used by the S μ MMIT XTE and the power planes used by the component performing a read access to the S μ MMIT XTE. The following example depicts the behavior seen in a system lacking common mode.

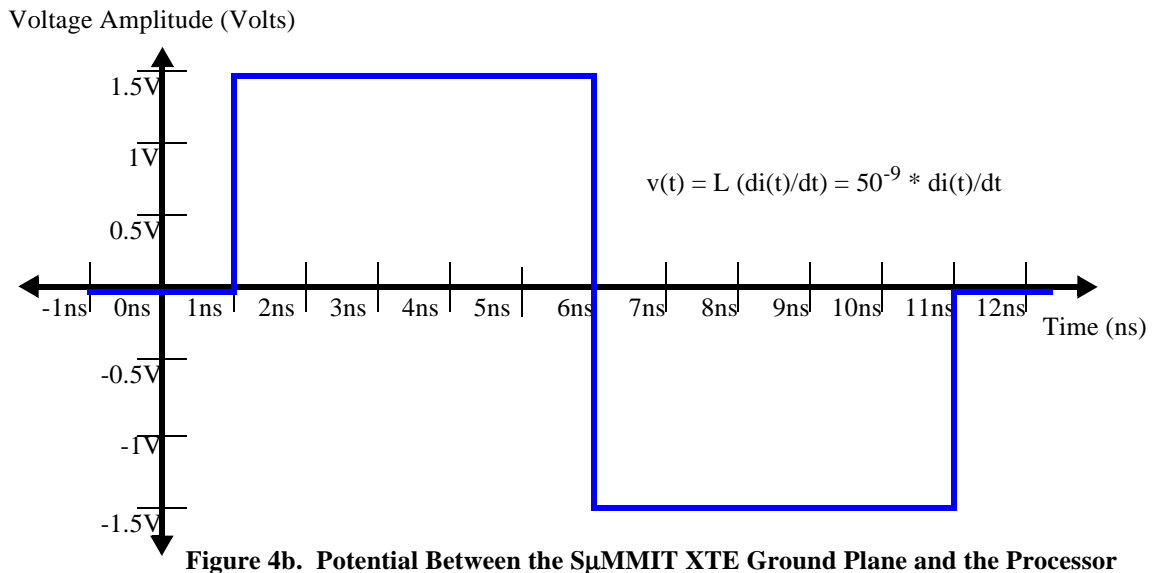
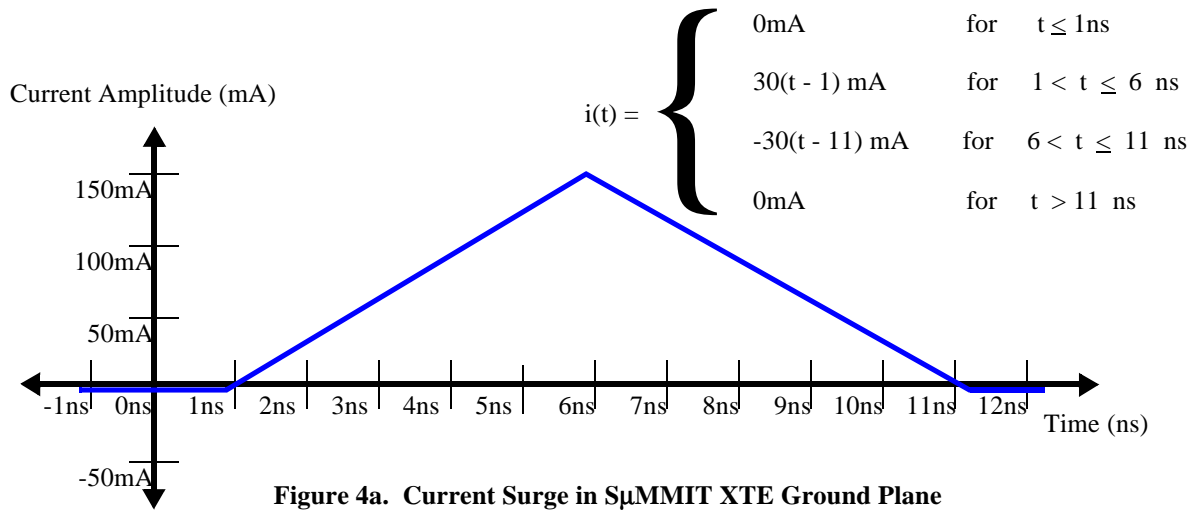
Given:

- 1) System architecture as depicted in Figure 1.
- 2) Inductance between the ground planes on each board is 50nH
(Includes inductance through edge connectors on each board and the backplane)
- 3) The excess current sunk from the SμMMIT XTE into its ground plane is shown in Figure 4a.

Note: The information shown in this example is theoretical and not taken from empirical or factual data.

Then:

- 1) The potential between the SμMMIT XTE ground plane and the Processor ground plane is shown in Figure 4b.



Using the above example, we can explain the reason for read failures to the SμMMIT XTE in systems lacking common mode between the SμMMIT XTE and the reading device. Specifically, a large potential difference between the ground plane used by the SμMMIT XTE and the ground plane used by the device performing a read results in the memory inputs to the SμMMIT XTE being sensed at invalid levels. As a result, the SμMMIT XTE quickly reacts to the “effective” change in state, resulting in bad data being latched at the SμMMIT XTE data outputs, or improper termination of the bus cycle as signaled by incorrect behavior of the RDY pin on the SμMMIT XTE. Figure 5 shows a noise margin diagram that can be used in conjunction with Table 2 to define the interface characteristics between the SμMMIT XTE and common buffer types.

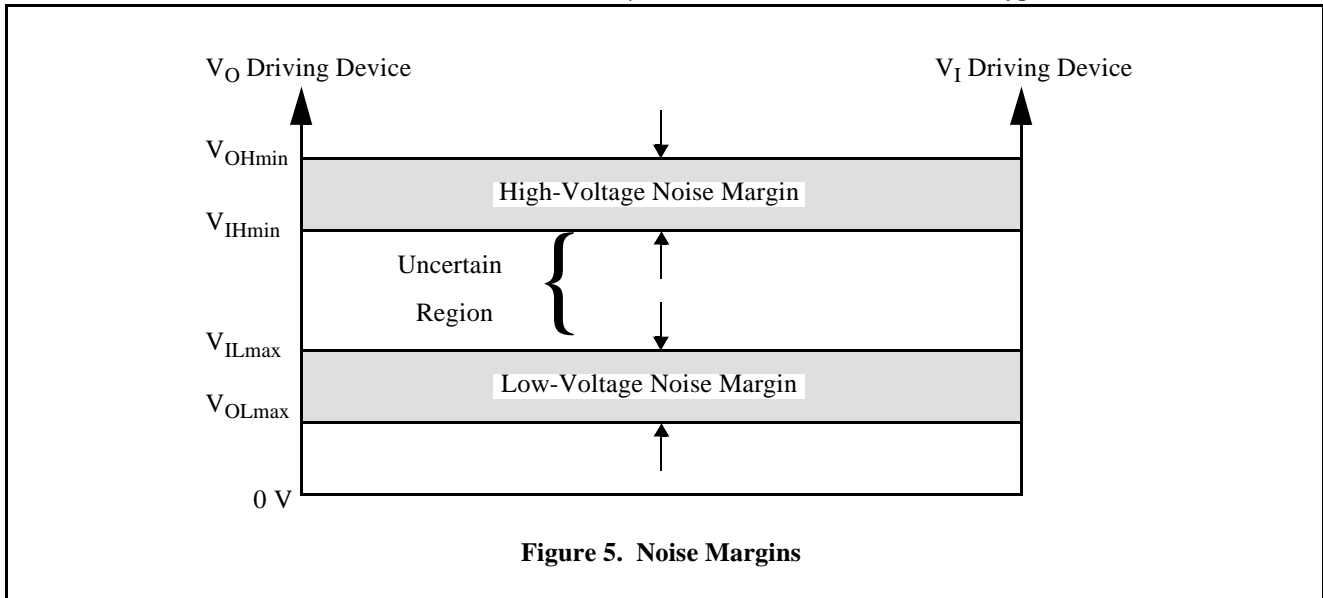


Table 2: Worst-Case Values of Primary Interfacing Parameters

Parameter	SμMMIT XTE	UT54ACS164245S Bus Transceiver	74HCMOS	AHC	74TTL	74LS	74AS	74ALS
V _{IHmin}	2.2 V	3.85 V	3.5 V	3.85 V	2 V	2 V	2 V	2 V
V _{ILmin}	0.8 V	1.65 V	1 V	1.65 V	0.8 V	0.8 V	0.8 V	0.8 V
V _{OHmin}	2.4 V	3.8 V	4.9 V	3.8 V	2.4 V	2.7 V	2.7 V	2.7 V
V _{OLmax}	0.4 V	0.4 V	0.1 V	0.44 V	0.4 V	0.4 V	0.4 V	0.4 V
I _{IHmax}	10 μA	3 μA	1 μA	1 μA	40 μA	20 μA	200 μA	20 μA
I _{ILmax}	-10 μA	-1 μA	-1 μA	-1 μA	-1.6 mA	-400 μA	-2 mA	-100 μA
I _{OHmax}	-4 mA	-8 mA	-4 mA	-8 mA	-400 μA	-400 μA	-2 mA	-400 μA
I _{OLmax}	4 mA	8 mA	4 mA	8 mA	16 mA	8 mA	20 mA	4 mA

Applying the data shown in Table 2 to the noise margin diagram in Figure 5, we can see that the S μ MMIT XTE has typical noise immunity of 0.4V typical on the low voltage side, and 0.2V to 2.7V of noise margin on the high voltage side depending on the device used to drive the S μ MMIT XTE. Extending this information to the ground bounce scenario described in Figure 4a and 4b, we notice when the S μ MMIT XTE ground plane drops 1.5V below the reading device's ground plane, then all low signals driven to the S μ MMIT XTE appear to be at least 1.5V. Referring to the noise margin diagram in Figure 5, an input of 1.5V to the S μ MMIT XTE falls into the "Uncertain Region." As a result, there is no guarantee how the S μ MMIT XTE evaluates the state of signals in this region. If, for example, the input falling into this "Uncertain Region" is a control signal (i.e. RD, CS, or DS), and the S μ MMIT XTE determines the signal is high, it would prematurely terminate the bus cycle. If, instead, the input falling into this "Uncertain Region" is an address input, and the S μ MMIT XTE determined the address input is high, it would fetch data from an incorrect address.

3.0 Techniques to Prevent Common Mode Failures

There are 3 primary methods to ensure that common mode failures do not occur when interfacing to the S μ MMIT XTE. The first, and most obvious, solution is to place the device initiating memory reads on the same module as the S μ MMIT XTE and ensure that both components share power and ground planes. The second preventative measure is to use schmitt triggered input buffers on the S μ MMIT XTE module. The third technique to minimize the risk of common mode failures is to latch the S μ MMIT XTE's memory interface inputs once they are received at the S μ MMIT XTE side of the system.

3.0.0 Local Integration to Prevent Common Mode Failures

The most certain method to ensure that your system does not exhibit any common mode failures is to design your system so that all fast source and destination components share power and ground planes. It is important to distinguish the term "source" refers to the devices that creates a signal, **not** the device that buffers/drives a signal to the destination. However, all devices in the signal lane from the source to the destination should share the same power and ground planes. The objective here is to reduce the inductive current path between the power/ground pins on the S μ MMIT XTE and the power/ground pins on the source component. By reducing the inductive current path between these pins, you ensure that both components have a very small potential between the corresponding power/ground pins on each part. As long as this potential between parts resides within the voltage noise margins depicted by Figure 5, then the S μ MMIT XTE will always evaluate low and high inputs correctly.

3.0.1 Schmitt Triggered Input Buffers to Prevent Common Mode Failures

If a system can not include the source and destination components on the same module and allow them to share the same power and ground planes, then the use of interface buffers offering schmitt triggered inputs like the UT54ACS164245S bus transceiver shown in Table 2 will facilitate an increased noise margin and could filter false signal transitions caused by ground bounce. The UT54ACS164245S has two major benefits. The first benefit is the large amount of noise margin for low signals. Specifically, the UT54ACS164245S ensures that an input of 1.65V or less will be driven out at 0.4V or less. The second benefit of the UT54ACS164245S is the schmitt triggered input technology which requires glitches to cross the V_{IH} or V_{IL} threshold in order to change state. This effectively removes the "Uncertain Region" shown in the noise margin diagram in Figure 5.

3.0.2 Input Latching to Prevent Common Mode Failures

An alternative method to the schmitt trigger solution described in section 3.0.1 of this document is to insert data latches between the S μ MMIT XTE and the backplane interface. Using a data latch for the relevant memory control signals and address bus inputs to the S μ MMIT XTE ensures the ground bounce exhibited during a S μ MMIT XTE read will be common moded with the S μ MMIT XTE and will not pass a signal glitch at the inputs of the latch. However, this solution is a little difficult to ensure that timing and clocking of the latches are sufficient to meet S μ MMIT XTE timing requirements and do not provide a false clock due to input glitches at the clock input to the latch.